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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,523	12/08/2003	Roger T. Clegg	03-1916	2973

7590 04/22/2005

LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
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EXAMINER

BUI, BRYAN

ART UNIT	PAPER NUMBER
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2863

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/730,523

Applicant(s)

CLEGG ET AL.

Examiner

Bryan Bui

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Wall et al (US 6,507,923).

With respect to claims 1, 10 and 19, Wall et al teach an integrated multi-channel Fibre channel analyzer provides coordinated and cooperative triggering and capturing of data cross multiple channel in the fibre channel network for testing the error handling capabilities of the system's firmware (abstract and column 6, lines 6-16) comprising defining a specific system event to be monitored (column 5, lines 34-40 and column 6, lines 16); creating a trigger in analyzer, wherein the trigger is used to allow the analyzer to capture information related to the specific system event (column 5, line 60 to column 6, line 6); receiving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed (abstract and column 2, line 31 to column 3, line 20 and column 5, line 60 to column 6, line 6).

With respect to claims 2-9, 11-18, 20-27, Wall et al teach the signal sent from one of a host system, a storage device, or peer communication device; the signal is sent from a fibre channel host bus adapter in the host system (column 3, lines 10-28); the analyzer is trigger within a millisecond of when the specific system event (error) occurs (column 6, lines 23-29); the analyzer is a FC (Fibre Channel) analyzer in column 4, lines 58+; th storage device includes initiators, target, switches or fabrics (column 8, line 65 to column 9, line 3); the Fibre channel host bus adapter includes a number of output pin and each pin output pin may be programmed with a separate triggering mechanism which include detection of device error, problem occur in device activity and input/ouput status (column 1, line 33 to column 2, line 16).

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-27 are rejected under 35 U.S.C. 102(a) as being anticipated by Wall et al (US 6,507,923).

With respect to claims 1, 10 and 19, Wall et al teach an integrated multi-channel Fibre channel analyzer provides coordinated and cooperative triggering and capturing of data cross multiple channel in the fibre channel network for testing the error handling capabilities of the system's firmware (abstract and column 6, lines 6-16) comprising defining a specific system event to be monitored (column 5, lines 34-40 and column 6, lines 16); creating a trigger in analyzer, wherein the trigger is used to allow the analyzer

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to capture information related to the specific system event (column 5, line 60 to column 6, line 6); receiving a signal at the analyzer, wherein the signal automatically triggers the analyzer to capture and store a predetermined amount of data related to the specific system event before and after the trigger is executed (abstract and column 2, line 31 to column 3, line 20 and column 5, line 60 to column 6, line 6).

With respect to claims 2-9, 11-18, 20-27, Wall et al teach the signal sent from one of a host system, a storage device, or peer communication device; the signal is sent from a fibre channel host bus adapter in the host system (column 3, lines 10-28); the analyzer is trigger within a millisecond of when the specific system event (error) occurs (column 6, lines 23-29); the analyzer is a FC (Fibre Channel) analyzer in column 4, lines 58+; th storage device includes initiators, target, switches or fabrics (column 8, line 65 to column 9, line 3); the Fibre channel host bus adapter includes a number of output pin and each pin output pin may be programmed with a separate triggering mechanism which include detection of device error, problem occur in device activity and input/ouput status (column 1, line 33 to column 2, line 16).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryan Bui whose telephone number is 571-272-2271. The examiner can normally be reached on M-Th from 7am-4pm, and Alternate Fridays.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BB

4/19/2005

BRYAN BUI
PRIMARY EXAMINER

